

The diagram illustrates a parallel processing system. At the top, two n -bit inputs are shown. The first input is connected to input 2a of a SUBTRACTER block (2). The second input is connected to input 2b of the same SUBTRACTER block. The SUBTRACTER block has two outputs: 2c, which is labeled 'D' and passes through an n -bit bus, and 2d, which is labeled 'F'. The output 'F' (2d) is connected to input 4a of an OR gate (4). The output 'D' (2c) is connected to input 4b of the OR gate. The output of the OR gate (4c) is connected to input 6b of a MUX block (6). The output 'D' (2c) is also connected to input 8b of a second MUX block (8). The output of the first MUX (6) is labeled 'c' (6c) and is connected to input 6a of the second MUX (8). The output of the second MUX (8) is labeled 'R' (8d) and passes through an n -bit bus. Control signals s1, s2, and s3 are shown entering the OR gate and the two MUX blocks respectively.

